



Quantum Digital Multimedia Card

General Description and Key Features

The Industrial Grades MMCplus is a removable flash card, measuring 24mm x 32mm x 1.4mm.

Quantum Digital's Industrial Grade MMCplus cards are specially designed, manufactured and tested to withstand extreme environmental conditions and to improve system reliability and endurance.

At the heart of each card, there is an advanced microcontroller that performs elaborate Flash management including 5-Bytes on-the-fly Error Detection and 4-Bytes Correction (EDC/ECC), bad block management (BBM) and extensive wear leveling.

Quantum Digital selects the highest reliability Single Level Cell (SLC) Flash for its superior endurance.

This combination allows achieving 2,000,000 logical program/erase cycles. The MMCplus has no moving parts inside. As such, it is made to withstand extreme shock and vibration.

Quantum Digital manufacturing process and test methodology makes the card even more robust. In fact, to assure that the cards shipped meets the rigorous threshold set by the OEM customers, each card is extensively tested at Quantum Digital's manufacturing facility to guarantee perfect functionality in any conditions. Quantum Digital provides rigorous bill of material control as an additional guarantee for the customer, ensuring long term product stability and availability. The MMCplus can be accessed through 2 interfaces. The card can operate in MMC mode or in SPI mode. While the MMC interface provides high performance with 1 bit, 4 bit, or 8 bit data transfer, the SPI mode allows easy integration in any type of application at lower performance.

Ordering Information: MMCplus Card

Ordering Information:

Part Number	Capacity
QDMMCP- 64MA(I)U	64 Mbytes
QDMMCP-128MA(I)U	128 Mbytes
QDMMCP-256MA(I)U	256 Mbytes
QDMMCP-512MA(I)U	512 Mbytes

(I) = Industrial temperature range (-40°C to +85 °C).

Part numbers without (I) = Commercial temperature range (0°C to 70°C).

Compliant to Specifications

- *MMC Specification v4.1

- *MMC Specification v3.3

Supports MMC Modes:

1 bit (default), 4 bit, and

8 bit

Supports SPI Mode

Variable Clock Rate:

- * Low frequency: 0 to 25MHz

- * High frequency: 0 MHz to 52MHz

Voltage Range: 2.7 to 3.6V

Low Power Consumption

Extended Data Write/Erase

Endurance

- * Optimized wear leveling algorithm

- * Hardware ECC to automatically detect and correct errors

- * 2,000,000 cycles

Data Retention: 10 years

Power-on damage free

card

insertion and removal

Two Operating

Temperature Ranges

available:

- * Commercial: 0 to 70°C

- * Industrial: -40 to 85°C

RoHS compliant lead-free

U = RoHS-6 compliant lead-free.

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1.0 Product Specifications

1.1 Package Dimensions and Pin Locations

Refer to the Table 1, and Figure 1 for package dimensions and pin locations of the card. Units are in millimeters, and tolerances are $\pm 0.15\text{mm}$ unless otherwise specified.

Table 1: Mechanical Dimensions MMCplus Card

Parameter	Value
Length	32.0 \pm 0.1mm
Width	24.0 \pm 0.08mm
Height	1.4 \pm 0.1mm

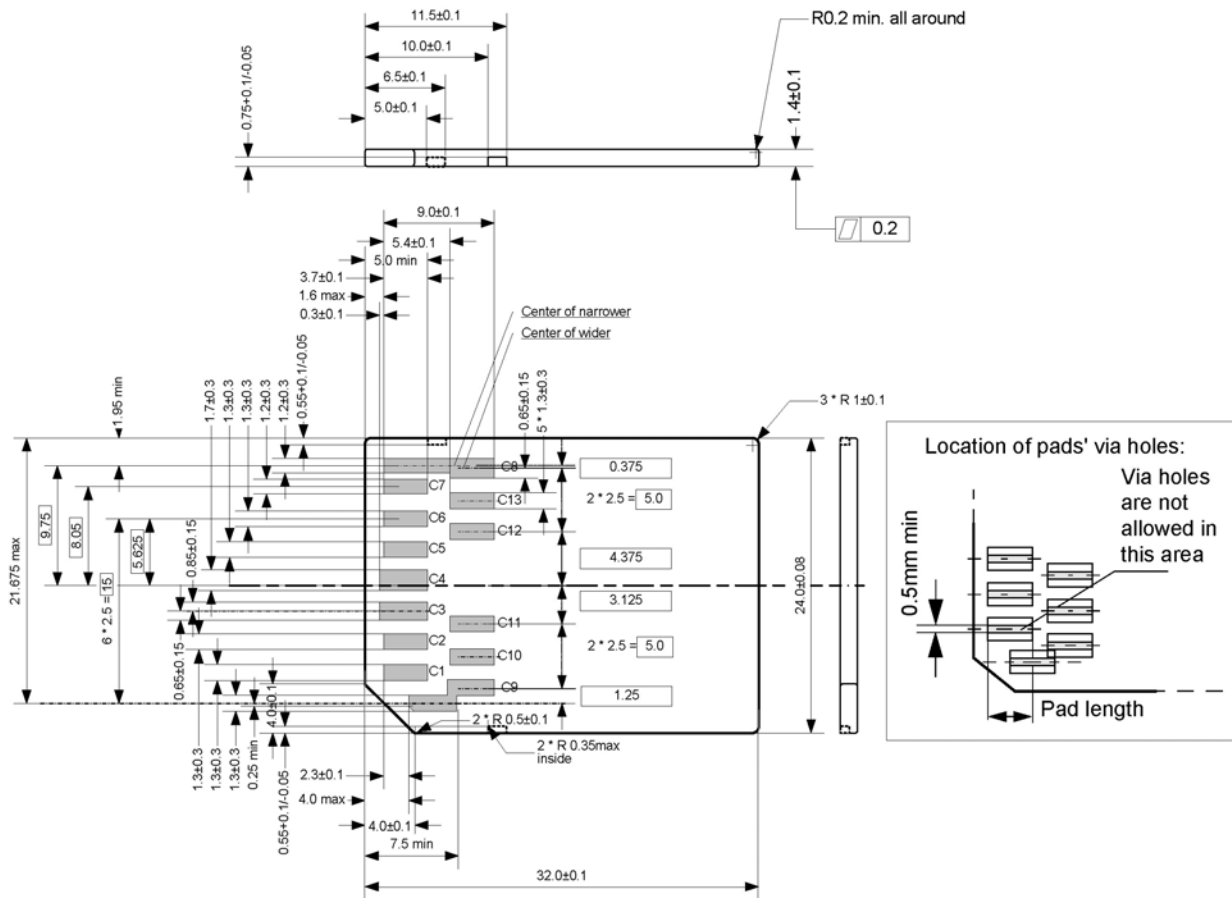


Figure 1: Mechanical Dimensions MMCplus Card

1.2 Pin Assignment and Signal Description

Table 2: MMCplus Card Pin Assignment and Signal Description

MMCplus Mode			
Pin	Signal Name	Pin Type	Description
1	DAT3	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 3.
2	CMD	Bi-directionally I/O, I/O using Push-Pull Drivers, Open Drain	Command/Response
3	VSS1	Supply	Supply voltage ground
4	VDD	Supply	Supply voltage
5	CLK	Input	Clock
6	VSS2	Supply	Supply voltage ground
7	DAT0	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 0.
8	DAT1	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 1.
9	DAT2	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 2.
10	DAT4	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 4.
11	DAT5	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 5.
12	DAT6	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 6.
13	DAT7	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 7.
SPI Mode			
Pin	Signal Name	Pin Type	Description
1	/CS	Input	Chip select (" <i>m</i> " indicates low active)
2	DI	Input	Data in
3	VSS1	Supply	Supply voltage ground
4	VDD	Supply	Supply voltage
5	SCLK	Input	Clock
6	VSS2	Supply	Supply voltage ground
7	DO	Output using Push Pull Drivers	Data out
8-13	—	—	Not used

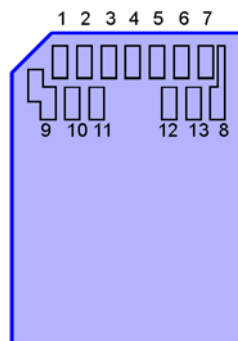


Figure 2: MMCplus Pin Locations

1.3 Performance

Measurements are in MMC bus mode using HB Bench test.

Table 3: MMCplus Card Read/Write Performance

Parameter	64MB	128MB	256MB	512MB	Unit
Sequential Read	Up to 8.6	Up to 11.1	Up to 11.1	Up to 11.1	Mbytes/s
Sequential Write	Up to 1.7	Up to 8.0	Up to 8.0	Up to 7.1	Mbytes/s
Random Read	Up to 8.3	Up to 10.6	Up to 10.7	Up to 10.7	Mbytes/s
Random Write	Up to 0.9	Up to 2.6	Up to 3.3	Up to 2.5	Mbytes/s

2.0 Environmental Specifications

2.1 Recommended Operating Conditions

Table 4: MMCplus Card Recommended Operating Conditions

Symbol	Parameter	Min	Type	Max	Unit
Ta	Commercial Operating Temperature	0	25	70	°C
	Industrial Operating Temperature	-40	-	85	°C
VDD	Supply Voltage	2.7	-	3.6	V
VSS1 VSS2	Supply Voltage Differentials	-0.5	-	0.5	V
-	Power Up Time (from 0V to VDD min)	-	-	250	ms

2.2 Reliability

Table 5: MMCplus Card Endurance & Data Retention

Parameter	Value
Endurance	2,000,000 Write/Erase Cycles
Data retention	10 years

2.3 Humidity & ESD

Table 6: MMCplus Card Shock, Vibration, Humidity & ESD

Parameter		Value
Humidity	Operating	25 °C/95% RH
	Storage	40°C/93% RH 500 hours
ESD	Contact Pad, Human Body Model According to ANSI EOS/ESD-S5.1-1998	>±4KV
	Non Contact Pad Area, Human body according to IEC61000-4-2 Coupling plane discharge	±8KV
	Air discharge	±15KV

3.0 Electrical Specifications

3.1 DC Characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 7: MMCplus Card DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Peak Voltage on all Lines	-0.5		3.6	V	VDD=3.3V
VIL	Input LOW Voltage			0.8	V	VDD=3.3V
VIH	Input HIGH Voltage	2.0			V	VDD=3.3V
VOL	Output LOW Voltage			0.4	V	VDD=3.3V
VOH	Output HIGH Voltage	2.4			V	VDD=3.3V
IDD	Operating Current			70	mA	VDD=3.3V
	Pre-initialization Standby Current			3	mA	VDD=3.3V
	Post-initialization Standby Current		110	150	µA	VDD=3.3V
ILI	Input Leakage Current	-1		1	µA	Without pull up R
IIO	Output Leakage Current	-1		1	µA	Without pull up R

3.2 Signal Loading

The total capacitance C_L of the CLK line of the MMC memory card bus is the sum of the bus master capacitance C_{HOST} , the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of the card connected to this line: $C_L = C_{HOST} + C_{BUS} + C_{CARD}$.

Requiring the sum of the host and bus capacitances not to exceed 20pF for the card, the values shown in Table 8 must not be exceeded.

Note: the total capacitance of CMD and DAT lines will be consist of C_{HOST} , C_{BUS} and one C_{CARD} only since they are connected separately to the MMC Memory Card host.

Table 8: MMCplus Card Signal Loading

Parameter	Symbol	Min	Max	Unit	Notes
Pull up resistance for CMD	R_{CMD}	4.7	100	K ohms	To prevent bus floating
Pull up resistance for DAT	R_{DAT}	50	100	K ohms	To prevent bus floating
Bus signal line capacitance	C_L		30	pF	Single card
Signal card capacitance	C_{CARD}		7	pF	Single card
Signal line inductance			16	nH	

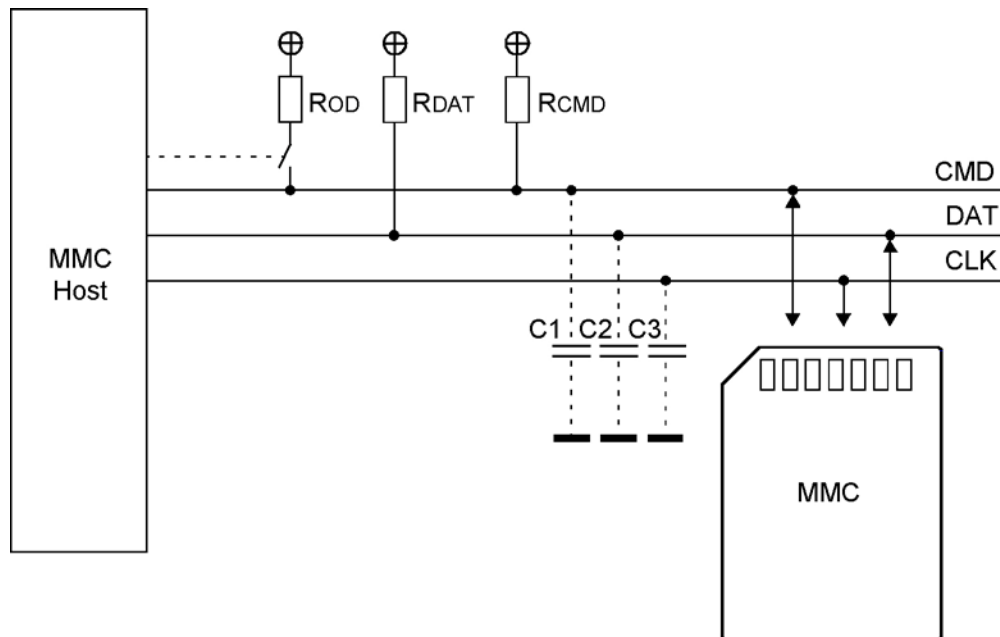


Figure 3: MMCplus Card Signal Loading

3.3 AC Characteristics

Table 9: AC Characteristics Low Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode	Fpp	0	25	MHz	Single card at $C_L \leq 30\text{pF}$
Clock frequency in card id mode	Fod	0	400	KHz	Single card at $C_L \leq 30\text{pF}$
Clock low time	tWL	10		ns	Single card at $C_L \leq 30\text{pF}$
Clock high time	tWH	10		ns	Single card at $C_L \leq 30\text{pF}$
Clock rise time	tTLH		10	ns	Single card at $C_L \leq 30\text{pF}$
Clock fall time	tTHL		10	ns	Single card at $C_L \leq 30\text{pF}$
CMD, DAT input setup time	tISU	3		ns	CMD,DAT Reference to CLK
CMD, DAT input hold time	tIH	3		ns	CMD,DAT Reference to CLK
Output delay time during Data Transfer Mode	tODLY	3	7	ns	CMD,DAT Reference to CLK

Notes:

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to V_{IH} min and V_{IL} max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

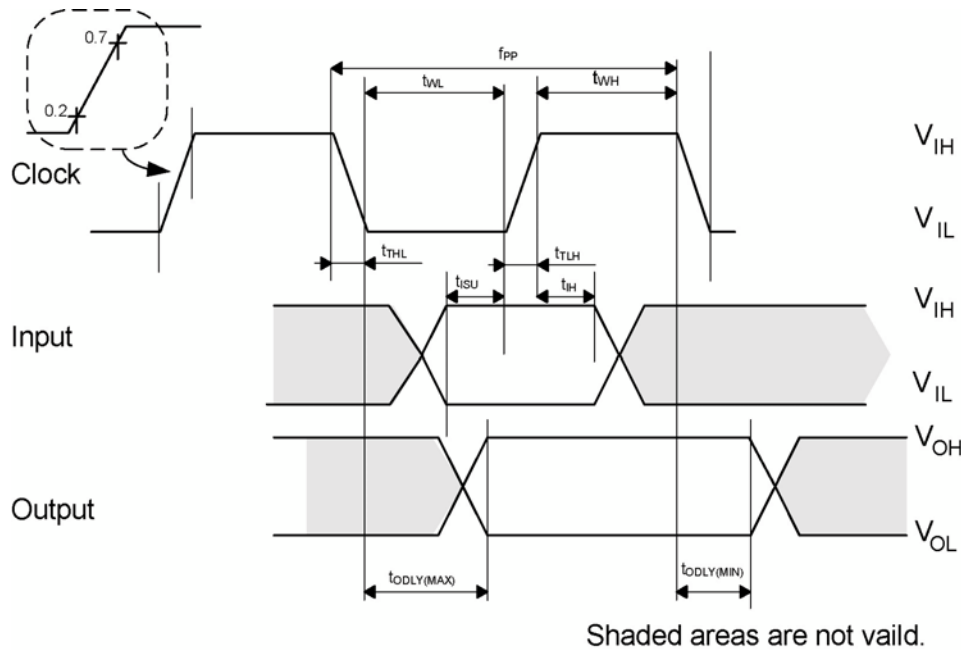


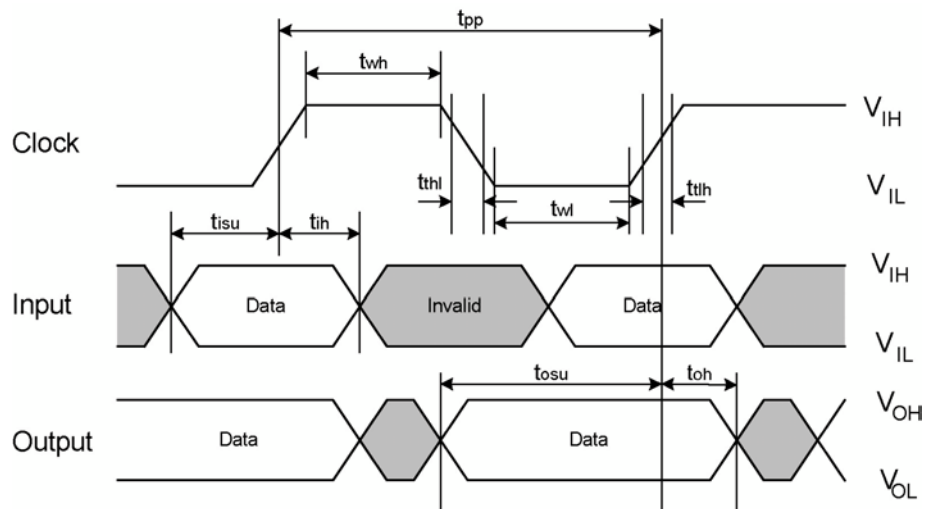
Figure 4: AC Characteristics Low Speed Mode

Table 10: AC Characteristics High Speed Mode

Parameter	Symbol	Min	Max	Unit
Clock frequency in data transfer mode	Fpp	26	52	MHz
Clock low time	tWL	6.5		ns
Clock high time	tWH	6.5		ns
Clock rise time	tTLH		3	ns
Clock fall time	tTHL		3	ns
CMD, DAT input setup time	tISU	3		ns
CMD, DAT input hold time	tIH	3		ns
CMD, DAT output setup time	tOSU	5		ns
CMD, DAT output hold time	tOH	6		ns
Signal rise time	tRISE		2.5	ns
Signal fall time	tFALL		2.5	ns

Notes:

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.
5. In order to satisfy severe timing, the host shall drive only one card. $C_L \leq 30\text{pF}$



Shaded areas are not valid.

Figure 5: AC Characteristics High Speed Mode

4.0 Host Access Specifications

The following chapters summarize how the host accesses the card:

- The block diagram in *Chapter 4.1* shows how the MMC and SPI buses interact with the registers via the controller.
- *Chapter 4.2* summarizes the MMC and SPI buses.
- *Chapter 4.2.3* summarizes the registers.

4.1 Functional Block Diagram

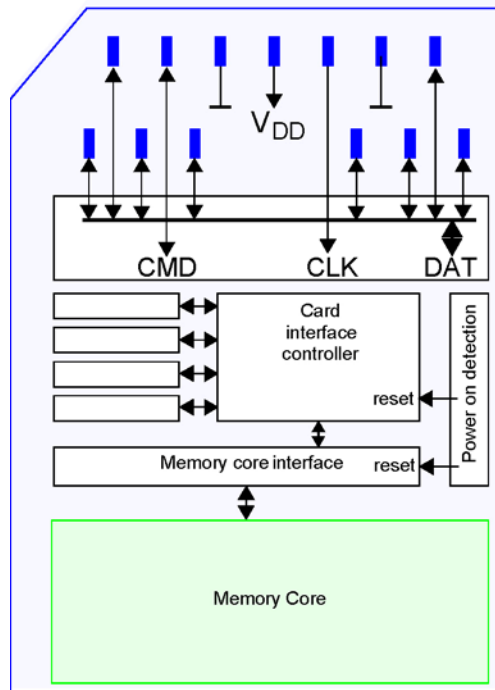


Figure 6: MMCplus Card Function Block Diagram

4.2 MMC and SPI Bus Modes

The card supports MMC and the SPI Bus modes. The host system can choose either one of the modes. The MMC mode uses a 1-bit, 4-bit, or 8 bit high performance data transfer, and the SPI mode provides secondary interface for compatibility to some lower performance MMC host systems.

4.2.1 MMC Bus Mode Protocol

The MMC Bus mode has a single master (host) and single slave (cards) synchronous topology.

The MMC bus signals are listed Table 11

Table 11: MMC Bus Signals

Signal	Description
CLK	Host to card clock signal
CMD	Bidirectional Command/Response signal
DAT0-DAT7	8 Bidirectional data signals
Vdd, Vss	Power and Ground

After a power-on reset, the host must initialize the card by a special message-based MultiMediaCard bus protocol.

Each message is represented by one of the following tokens:

- Command: a command is a token which starts an operation. A command is sent from the host to a card. A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from the card to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

The number of data lines used for the data transfer can be 1(DAT0), 4(DAT0-DAT3) or 8(DAT0-DAT7).

Card addressing is implemented using a session address, assigned during the initialization phase, by the bus controller to the connected card. A card is identified by its CID number.

4.2.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.

While the MultiMediaCard channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed Table 12.

Table 12: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
SCLK	Host to card clock signal
Data In (DI)	Host to card data signal
Data Out (DO)	Card to host data signal
Vdd, Vss	Power and ground

4.2.3 Mode Selection

The MultiMediaCard wakes up in the MultiMediaCard mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0). Selecting SPI mode is not restricted to Idle state (the state the card enters after power up) only. Every time the card receives CMD0, including while in Inactive state, CS signal is sampled.

If the card recognizes that the MultiMediaCard mode is required (CS signal is high), it will not respond to the command and remain in the MultiMediaCard mode. If SPI mode is required (CS signal is low), the card will switch to SPI and respond with the SPI mode R1 response.

The only way to return to the MultiMediaCard mode is by a power cycle (turn the power off and on). In SPI mode, the MultiMediaCard protocol state machine is not observed. All the MultiMediaCard commands supported in SPI mode are always available.

4.3 Card Registers

The MMCplus Card has six registers. Refer to Tables 13 to 17 for details.

Table 13: MMCplus Card Register

Register Name	Byte Width	Description	Function
CID	16	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	4	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	16	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD(CMD27).
RCA	2	Relative Card Address	This register carries the card address in MMC Card mode.
Ext_CSD	512	Extended Card Specific Data	This register provides an optional function for the output driver condition.
DSR	16	Driver Stage Register	This register provides an optional function for the output driver condition and is not implemented in this card.

Table 14: CID Register

Register Name	Bit Width	CID-slice	Description
MID	8	[127:120]	Manufacture ID
OID	16	[119:104]	OEM/Application ID
PNM	48	[103:56]	Product Name
PRV	8	[55:48]	Product Version
PSN	32	[47:16]	Product Serial Number
MDT	8	[15:8]	Manufacture Date
CRC	7	[7:1]	Check sum of CID contents
—	1	[0:0]	Not used; always=1

Table 15: OCR Register

OCR bit position	VDD voltage window	Value	OCR bit position	VDD voltage window	Value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24-30	Reserved	1
13	2.5-2.6	0	31	Card power up status bit (busy)	0=busy; 1=ready
14	2.6-2.7	0			

Table 1616: CSD Register for MMC v4.0

Register Name	Byte Width	Cell Type	CSD slice	Value	Note	Description
CSD_STRUCTURE	2	R	[127:126]	11b	Higher than v3.3	CSD structure
SPEC_VERS	4	R	[125:122]	0100b	V4.0	Specification version
—	6	R	[121:120]	—	—	Reserved
TAAC	8	R	[121:112]	7Fh	80ms	Data read access time 1
NSAC	8	R	[111:104]	FFh	25.5k clocks	Data read access time 2 (CLK cycle)
TRAN_SPEED	8	R	[103:96]	2Ah	20 MHz	Data transfer rate
CCC	12	R	[95:84]	0F5h	Class 0,2,4,5,6,7 supported. Class 1,3,8 not supported.	Card command classes
READ_BL_LEN	4	R	[83:80]	9h	512 bytes	Read data block length
READ_BL_PARTIAL	1	R	[79:79]	1b	Supported	Partial blocks for read allowed
WRITE_BLK_MISALIGN	1	R	[78:78]	1b	Supported	Write block misalignment
READ_BLK_MISALIGN	1	R	[77:77]	1b	Supported	Read block misalignment
DSR_IMP	1	R	[76:76]	0b	Not supported	DSR implemented
—	2	R	[75:74]	—	—	Reserved
C_SIZE	12	R	[73:62]	Varies	—	Device size
VDD_R_CURR_MIN	3	R	[61:59]	101b	35mA	VDD min read current
VDD_R_CURR_MAX	3	R	[58:56]	101b	45mA	VDD max read current
VDD_W_CURR_MIN	3	R	[55:53]	101b	35mA	VDD min write current
VDD_W_CURR_MAX	3	R	[52:50]	101b	45mA	VDD max write current
C_SIZE_MULT	3	R	[49:47]	Varies.	—	Device size multiplier
ERASE_GRP_SIZE	5	R	[46:42]	Varies	—	Erase group size
ERASE_GRP_SIZE_MULT	5	R	[41:37]	Varies	—	Erase group size multiplier
WP_GRP_SIZE	5	R	[36:32]	Varies	—	Write protect group size
WP_GRP_ENABLE	1	R	[31:31]	1b	Supported	Write protect group enable
—	2	R	[30:29]	00b	None	Reserved
R2W_FACTOR	3	R	[28:26]	101b	32X	Write speed factor
WRITE_BL_LEN	4	R	[25:22]	9h	512 bytes	Write data block length
WRITE_BL_PARTIAL	1	R	[21:21]	1b	Supported	Partial block write allowed
—	4	R	[20:17]	—	—	Reserved
CONTENT_PROT_APP	1	R	[16:16]	0b	Not supported	
FILE_FORMAT_GRP	1	R/W	[15:15]	0b	HD like FAT	File format group
COPY	1	R/W	[14:14]	0b	Not copied	Copy flag
PERM_WRITE_PROTECT	1	R/W	[13:13]	0b	Not protected	Permanent write protection
TMP_WRITE_PROTECT	1	R/W	[12:12]	0b	Not protected	Temporary write protection
FILE_FORMAT	2	R/W	[11:10]	00b	HD like FAT	File format
—	2	R/W	[9:8]	00b	None	Reserved
CRC	7	R/W	[7:1]	(CRC)	—	Checksum of CSD contents
—	1	-	[0:0]	1b	—	Always=1

Table 177: Ext_CSD Register for MMC v4.0

Register Name	Byte Width	Ext_CSD Slice	Value	Note	Description
Properties Segment					
—	7	[511:505]	—	—	Reserved
S_CMD_SET (R)	1	[504]	00h	Standard MMC	Supported command sets
—	300	[503:204]	—	—	Reserved
PWR_CL_26_360 (R)	1	[203]	—	Not finalized	Power class for 26MHz@3.6V
PWR_CL_52_360 (R)	1	[202]	—	Not finalized	Power class for 52MHz@3.6V
PWR_CL_26_195 (R)	1	[201]	—	Not finalized	Power class for 26MHz@1.95V
PWR_CL_52_195 (R)	1	[200]	—	Not finalized	Power class for 52MHz@1.95V
—	3	[199:197]	—	—	Reserved—
CARD_TYPE (R)	1	[196]	03h	HS-MMC@52MHz	Card type
—	1	[195]	—	—	Reserved
CSD_STRUCTURE (R)	1	[194]	03h	v4.0	CSD structure version
—	1	[193]	—	—	Reserved
EXT_CSD_REV (R)	1	[192]	00h	Revision1.0	Extension CSD Reversion
Modes Segment					
CMD_SET (R/W)	1	[191]	Set up by host	—	Command set
—	1	[190]	—	—	Reserved
CMD_SET_REV (RO)	1	[189]	00h	v4.0	Command set revision
—	1	[188]	—	—	Reserved
POWER_CLASS (R/W)	1	[187]	Set up by host	—	Power class
—	1	[186]	—	—	Reserved
HS_TIMING (R/W)	1	[185]	Set up by host	—	High speed interface timing
—	1	[184]	—	—	Reserved
BUS_WIDTH (WO)	1	[183]	Set up by host	—	Bus width mode
—	183	[182:0]	—	—	Reserved