Quantum Digital Flash Drive

General Description and Key Features

Quantum Digital's flash storage complies with industry's standards and global regulatory compliance. Each device incorporates a proprietary flash controller and SLC Samsung Nand Flash Memory that provides the greatest flexibility to customer - specific applications while supporting key flash management features resulting in the industry's highest reliability and endurance Key features include:

Built-in ECC engine detects up to 5-byte and corrects up to 4- byte errors.
Sophisticated block management and wear leveling algorithms guarantees 4,000,000 write/erase cycles.
Power-down data protection ensures data integrity and errors in case of power loss Lifecycle management feature allows users to monitor the device's block management.

Quantum Digital's 2.5" IDE Flash Drive is the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, ESD, and temperature. The rugged industrial design combined with industrial temperature (-40°C to 85°C) testing and adherence to rigid JEDEC JESD22 standards ensures flawless execution in the harshest environments. In addition to custom hardware and firmware designs, Quantum Digital also offers value-added services including:

- Custom labeling and packaging.
- Custom software imaging and ID strings.
- Full BOM control and product change notification
- Total supply-chain management to ensure continuity of supply.
- In-field application engineering to help customers through product designing

Solid - State IDE Flash Drive (No Moving Parts)
Capacity: 128 MB -16 GB
ATA - 5 Compatible
ATA Transfer modes: PIO 0 -6, MWDMA 0-4
Supports True IDE and PC Card Memory and I/O Modes
Form Factors: 2.5-inch Ruggedized Enclosure with 44-pin IDE Connector
Endurance Guarantee of 4,000,000 Write/Erase Cycles
Master or Slave Select by Jumper
5V or 3.3V Power Supply
Commercial and Industrial Operating Temperature Range
5-Byte Detection, 4-Byte Correction ECC Engine
10 Year Data Retention
RoHS-6 Compliant

Ordering Information: IDE Flash Drive

Ordering Information:

Part Number	Form Factor	Capacity
QDFLD25-128MUH1(I)	2.5-inch/44-pin	128 Mbytes
QDFLD25-256MUH1(I)	2.5-inch/44-pin	256 Mbytes
QDFLD25-512MUH1(I)	2.5-inch/44-pin	512 Mbytes
QDFLD25-1GUH1(I)	2.5-inch/44-pin	1 GByte
QDFLD25-2GUH1(I)	2.5-inch/44-pin	2 GBytes
QDFLD25-4GUH1(I)	2.5-inch/44-pin	4 GBytes
QDFLD25-8GUH1(I)	2.5-inch/44-pin	8 GBytes
QDFLD25-16GUH1(I)	2.5-inch/44-pin	16 GBytes

QDFLD = QDT standard 2.5” IDE Flash Drive part number prefix.

25 = 2.5-inch form factor.

(M/G) = proceeding capacity (xxx) is in Megabytes (M) or Gigabytes (G).

H1 = QDT H1 controller.

U = RoHS-6 compliant lead-free.

Part numbers without (I) = Commercial temperature range (0ºC to 70ºC).

(I) = Industrial temperature range (-40ºC to +85 ºC).

F = media set to fixed storage for non - removable IDE applications. Use with operating systems, such as Windows XP, that require storage media to be identified as a fixed drive before it can be used as a bootable drive.

CONTENTS

1. Introduction

The Industrial 2.5" PATA (IDE) SSD products are designed to follow ATA/ATAPI-6 standard. The main used Flash memories are Samsung SLC-NAND Type Flash memory chips from 128MB up to 8GB, and Micron SLC-NAND Type Flash memory chips for 16GB only. The operating temperature grade is optional for standard grade 0°C ~ 70°C and industrial grade -40°C ~ +85°C. The Industrial 2.5" PATA (IDE) SSD are designed electrically compliant with the conventional IDE hard disk and support True IDE Mode. The data transfer modes supports PIO 0~4, MWDMA 0~2, or UDMA 0~4; Default setting are PIO mode-4 or UDMA-4. 2.5" PATA (IDE) SSD features an extremely light weight, reliable, low-profile form factor.

The Industrial 2.5" PATA (IDE) SSD provides a high level interface to the host computer. This interface allows a host computer to issue commands to the SSD to read or write blocks of memory. The host addresses the card in 512 byte sectors. Each sector is protected by a powerful 4 bits Error Correcting Code (ECC). The Industrial 2.5" PATA (IDE) SSD, it uses intelligent controller which manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech Industrial 2.5" PATA (IDE) SSD controller.

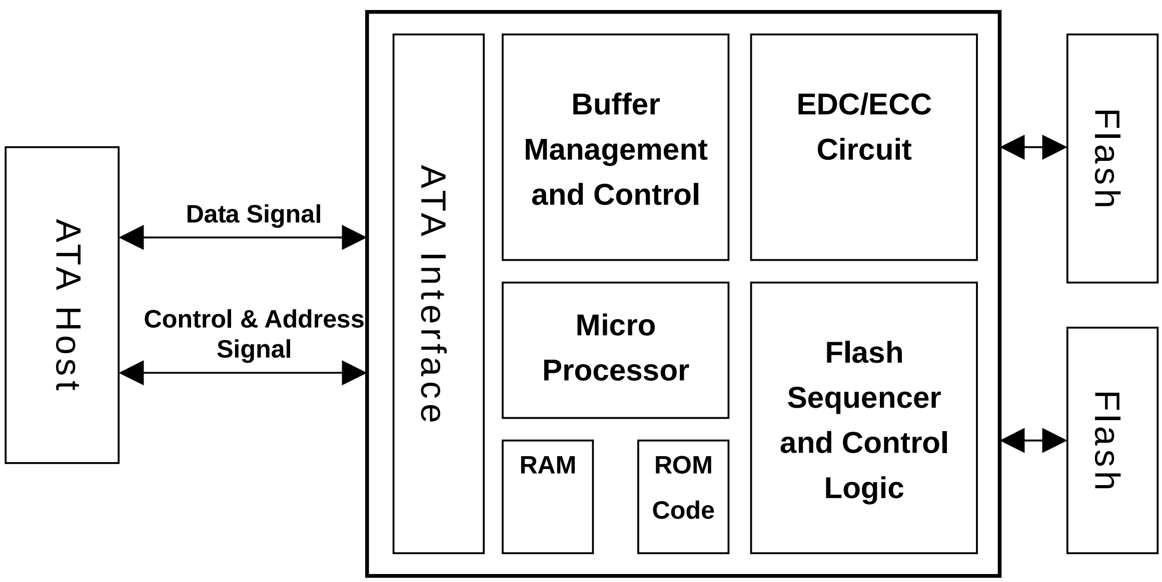

Figure 1: 2.5" PATA (IDE) SSD Controller Block Diagram

1.1. *Scope*

This document describes the features and specifications and installation guide of the Industrial 2.5” PATA (IDE) SSD.

1.2. *System Features*

- Non-volatile memory and no moving parts
- SLC NAND type flash technology
- 2.5” IDE drive form-factor
- Extremely rugged metal casing to endure harsh environments
- Disk capacity from 128MB to 16GB
- ATA interface and True IDE mode
- Master/Slave Switch
- Data transfer supports PIO-4 and UDMA-4 (Default setting)
- Performance up to 40.0MB/sec
- Automatic 4 bits error correction and retry capabilities
- Supports power down commands and Auto stand-by / sleep modes.
- +5 V ±10% operation
- Working well in critical environment
- Very high performance, very low power consumption
- Low weight, Noiseless
- Optional for conformal-coating special PCB surface coating treatment

1.3. *ATA/ATAPI-6 Standard*

The Industrial 2.5” PATA (IDE) SSD disks are fully compatible with the ATA/ATAPI-6 standard.

1.4. *Technology Independence - Static Wear Leveling*

In order to gain the best management for flash memory, the Industrial Rugged Metal 2.5” PATA (IDE) SSD supports ***Static Wear-leveling technology*** to manage the Flash system. The life of flash memory is limited; the management is to increase the life of the flash product.

A static wear-leveling algorithm evenly distributes data over an entire Flash cell array and searches for the least used physical blocks. The identified low cycled sectors are used to write the data to those locations. If blocks are empty, the write occurs normally. If blocks contain static data, it moves that data to a more heavily used location before it moves the newly written data. The static wear leveling maximizes effective endurance Flash array compared to no wear leveling or dynamic wear leveling.

1.5. *Conformal coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. We apply only silicone on our storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

We use MIL-I-46058C silicon conformal coating.

2. *Product Specifications*

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. *System Environmental Specifications*

Table 1: Environmental Specification

The Industrial 2.5" PATA (IDE) SSD		Standard Grade	Industrial Grade
Temperature	**Operating:** **Non-operating:**	0ºC ~ +70ºC -20ºC ~ +80ºC	-40ºC ~ +85ºC -50ºC ~ +95ºC
Humidity	**Operating & Non-operating:**	10% ~ 95% non-condensing	
Vibration	**Operating & Non-operating:**	15G compliance to MIL-STD-810F	
Shock	**Operating & Non-operating:**	1,500G compliance to MIL-STD-810F	
Altitude	**Operating & Non-operating:**	70,000 feet	

2.2. *System Power Requirements*

Table 2: Power Requirement

The Industrial 2.5" PATA (IDE) SSD		Standard Grade	Industrial Grade
DC Input Voltage (VCC) 100mV max. ripple(p-p)		**+5 V ±10%**	
+5V Current **(Maximum average value)**	**Reading Mode :**	124.0 mA (Max.)	
	Writing Mode :	121.0 mA (Max.)	
	Idle Mode :	1.8 mA (Max.)	

2.3. *System Performance*

Table 3: System Performances

Data Transfer Mode supporting		- PIO mode: 0,1,2,3,4, (Default PIO-4) - MWDMA mode: 0,2 - UDMA Mode: 0,1,2,3,4 (Default UDMA-4)
Data Transfer Rate To/Form Host		16.6Mybtes/sec burst under PIO Mode 4 66.6Mbytes/sec burst under UDMA-4 Mode
Average Access Time		0.2 ms(estimated)
Maximum Performance	**Sequential Read**	40 Mbytes/sec Max.
	Sequential Write	20 Mbytes/sec Max.

Note:

(1). All values quoted are typically at 25oC and nominal supply voltage.

(2). Testing of the Industrial 2.5" PATA (IDE) SSD maximum performance was performed under the following platform:

- Computer with AMD 3.0GHz processor

- Windows XP Professional operating system

- IDE transfer mode: Ultra DMA mode 4

- PATA (IDE) SSD capacity: 4GB

2.4. *System Reliability*

Table 4: System Reliability

MTBF	>3,000,000 hours
Wear-leveling Algorithms	Static Wear Leveling
ECC Technology	4 bits per 512 bytes block
Endurance	Greater than 2,000,000 cycles Logically contributed by Wear-leveling and advanced bad sector management
Data Retention	10 years

2.5. *Physical Specifications*

Refer to Table 5 and see Figure 2 for Industrial 2.5" PATA (IDE) SSD physical specifications and dimensions.

Table 5: Physical Specifications

2.5" PATA (IDE) SSD	
Length:	99.70 ± 0.25mm(4.0 ± 0.010 in)
Width:	69.9 ± 0.25mm(2.76 ± 0.1.010 in)
Thickness:	9.5 ± 0.25mm(0.4 ± 0.010 in)
G. W. :	115g (4.6oz)

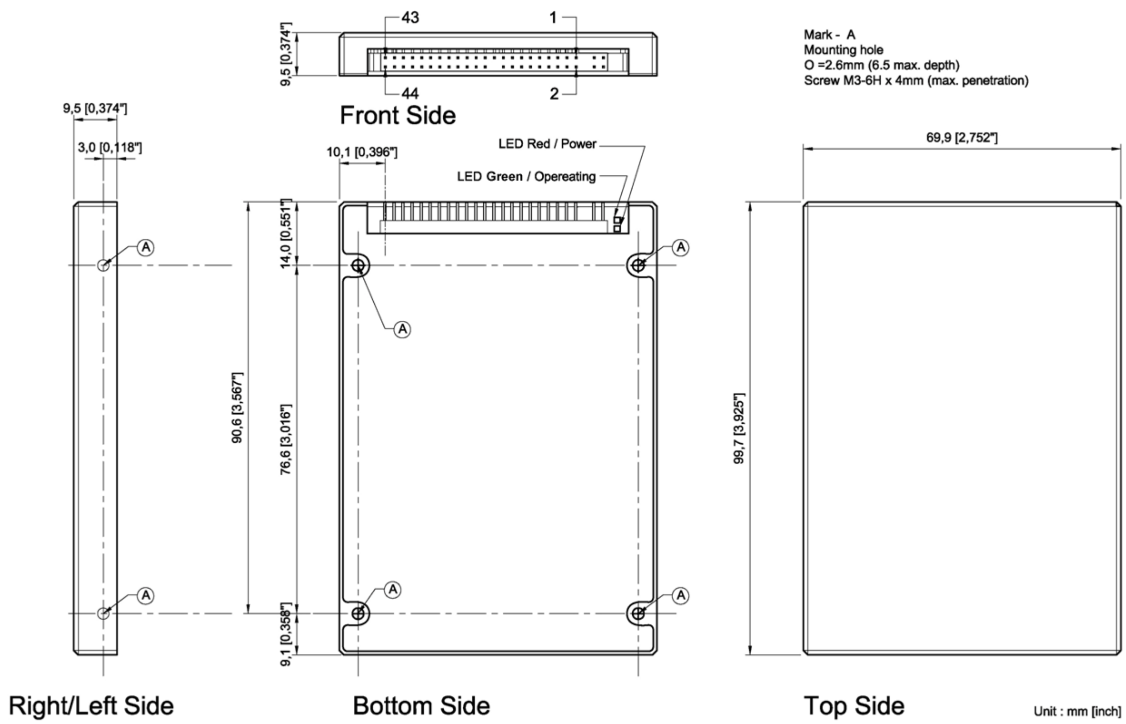

Figure 2: 2.5" PATA (IDE) SSD

2.6. *Capacity Specifications*

The table 6 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 6: Device Parameter

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	Default CHS Capacity
128MB	497	16	32	254,464
256MB	984	16	32	503,808
512MB	1,001	16	63	1,009,008
1,024MB	2,002	16	63	2,018,016
2.04GB	4,003	16	63	4,035,024
4GB	8,006	16	63	8,070,048
8GB	16,000	16	63	16,128,000
16GB	32,235	16	63	32,492,880

3. *Interface Description*

3.1. *Physical Description*

The pin 1 ~ pin 44 are for IDE interface. The pin A ~ pin D are for option selection via physical jumpers.

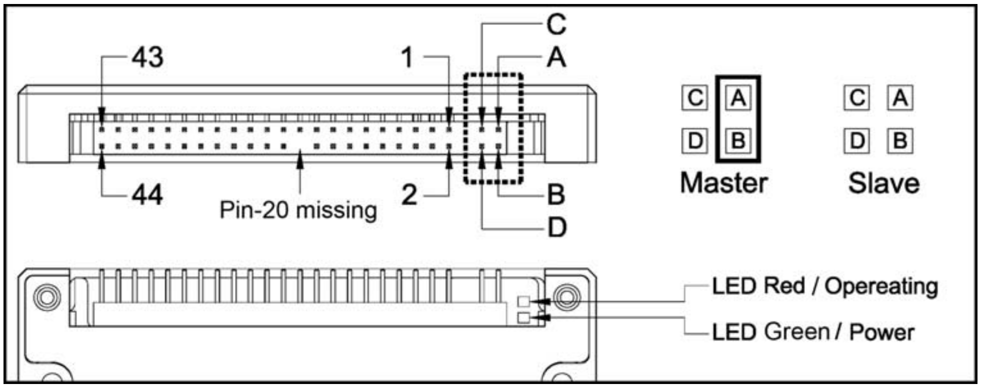

Figure 3: The front view of 2.5" PATA (IDE) SSD 44-pin IDE Connector

3.2. *Pin Assignments*

Signals whose source is the host is designated as inputs while signals that the Industrial 44-pin micro IDE Flash (2.5" PATA (IDE) SSD) Disk sources are outputs. The pin assignments are listed in below table 7.

Table 7: Pin Assignments

Pin No.	Signal Name	Description	Pin No.	Pin Name	Description
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	KEY[1]	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
23	HIOW[3]	Host I/O Write	24	24	GND
	STOP[4]	Stop Ultra DMA burst			
25	HIOR[3]	Host I/O Read	26	GND	Ground
	HDMARDY[4]	Ultra DMA ready			
	HSTROBE[4]	Ultra DMA data strobe			
27	IORDY[3]	I/O Ready	28	CSEL	Cable select
	DDMARDY[4]	Ultra DMA ready			
	DSTROBE[4]	Ultra DMA data strobe			

29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41	VCC	Supply Voltage	42	VCC	Supply Voltage
43	GND	Ground	44[2]	NC	Not Connected

In the 44-pin version, this pin is defined as KEY, according to the ATA standard.

NC = These pins are not connected internally.

Signal usage in PIO & Multiword DMA mode.

Signal usage in Ultra DMA mode.

3.3. *Electrical Description*

The Industrial 2.5" PATA (IDE) SSD is optimized for operation with hosts. Table 8 describes the signals of 44-pin IDE interface.

Table 8: Signal Description

Pin No.	Signal Name	Type	Description
1	HRESET-	I	Host reset signal, High: Reset.
37	CS0-	I	Chip select CS0
38	CS1-	I	Chip select CS1
31	INTRQ	O	Host interrupt signal.
25	HIOR-[3]	I	I/O read strobe signal.
	HDMARDY-[4]		DMA ready during Ultra DMA data in burst
	HSTROBE[4]		Data strobe during Ultra DMA data out burst
23	HIOW-[3]	I	I/O write strobe signal.
	STOP[4]		Stop during Ultra DMA data bursts
32	IOCS16-	O	Asserted in 16-bit access.
27	IORDY[3]	O	I/O Ready Signal
	DDMARDY-[4]		DMA ready during Ultra DMA data out burst
	DSTROBE[4]		Data strobe during Ultra DMA data in burst
18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	HDB[15:0]	I/O	Host data bus
33, 35, 36	HAB[2:0]	I/O	Host Address bus
28	CSEL- I	I	Master/Slave select signal (cable select signal). Low: Device operates as a master, High: Device operates as a slave. Switch used.
39	DASP-	I/O	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.

34	PDIAG-	I/O	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.
21	DMARQ	O	DMA Request.
29	DMACK-	I	DMA Acknowledge.
20[1], 41[2], 42[2]	VCC	VCC	Connect to VCC
2, 19, 22, 24, 26, 30, 40, 43[2]	GND	GND	Connect to GND.
44[2]	NC	N/A	Not used. Please do not connect.

In the 44-pin version, this pin is defined as KEY, according to the ATA standard.

NC = These pins are not connected internally.

Signal usage in PIO & Multiword DMA mode

Signal usage in Ultra DMA mode

3.4. *Electrical Specification*

Table 10, Table 11, and Table 12 defines all D.C. Characteristics for the Industrial 2.5" PATA (IDE) SSD. Unless otherwise stated, a condition is as below Table 9:

Table 9: Electrical Condition

Standard Grade	Industrial Grade
Vcch = 5V ±10% Ta = 0°C to 70°C	Vcch = 5V ±10% Ta = -40°C to 85°C

3.4.1. Absolute Maximum Rating

Table 10: Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
DC Power Supply	V_{DD} - V_{SS}	-0.3 ~ +5.5	V
Input voltage	V_{IN}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Operating Temperature	T_A	Standard: -10 ~ +70	°C
		Industrial: -40 ~ +85	°C
Storage Temperature	T_{ST}	Standard: -20 ~ +80	°C
		Industrial: -50 ~ +95	°C

3.4.2. Recommended Operating Condition

Table 11: Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	Vcc	3.0	3.3	3.6	V
Input Voltage	V_{IN}	-0.3	-	Vcc+0.3	V
Power Supply for Host I/O	Vccq	3.0	-	5.5	V
Input Voltage for Host I/O	V_{IN_Host}	-0.3	-	Vccq+0.3	V

3.4.3. DC Characteristics

Table 12: DC Characteristics

Parameter	Symbol	Value			Unit
		Min	Standard	Max	
Power Supply	VCCH	4.5	5.0	5.5	V
Power Supply	VCCF	3.0	3.3	3.6	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input high voltage	V_{IH}	2.0		Vcc+0.3	V
Output low voltage	V_{OL}			0.45 (at 4mA)	V
Output high voltage	V_{OH}	2.4 (at 1mA)			V
Operating CurrentV Sleep Mode Operation	Icc			 1.4 140	 mA mA
Input Leakage Current	ILI			±10	uA
Output leakage current	L_{LO}			±10	μA
Input/output Capacitance	$C_{I/O}$			10	pF

3.4.4. Timing Specifications

PIO Mode

Figure 4: Read/Write Timing Diagram, PIO Mode

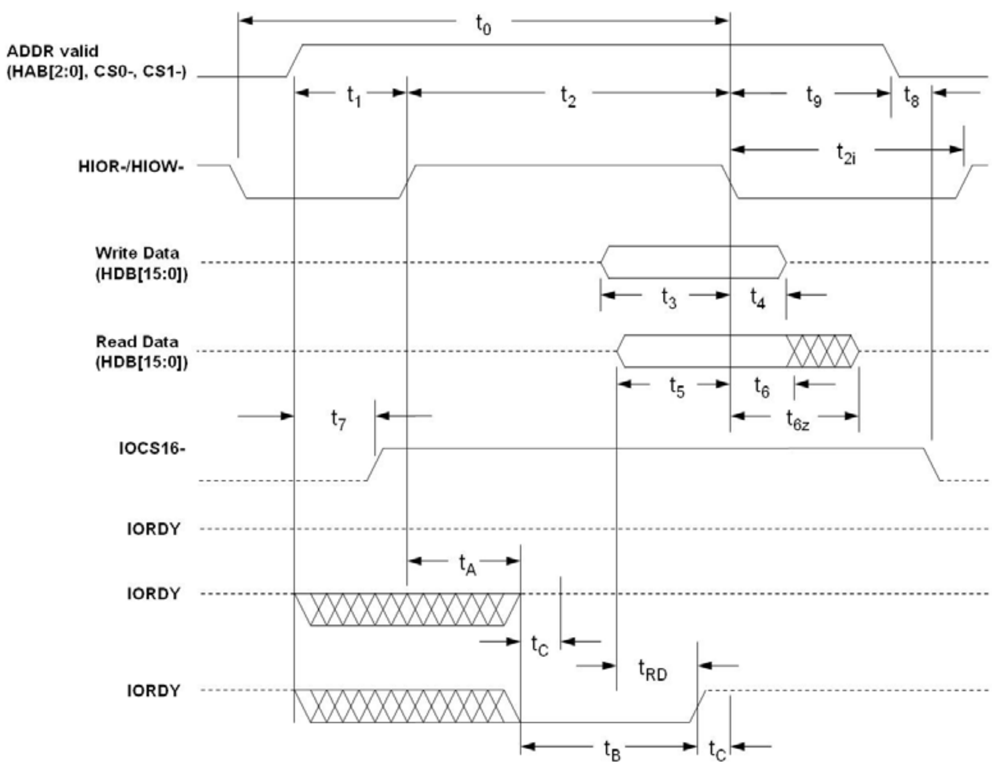

Table 13: Read/Write Timing Specifications, PIO Mode 0-4

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	600	383	240	180	120
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t_2	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25
t_3	HIOW- data setup (min.)	60	45	30	30	20
t_4	HIOW- data hold (min.)	30	20	15	10	10
t_5	HIOR- data setup (min.)	50	35	20	20	20
t_6	HIOR- data hold (min.)	5	5	5	5	5
t_{6z}	HIOR- data tri-state (max.)	30	30	30	30	30
t_7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a
t_8	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max.)	5	5	5	5	5

Multiword DMA

Figure 5: Read/Write Timing Diagram, Multiword DMA Mode

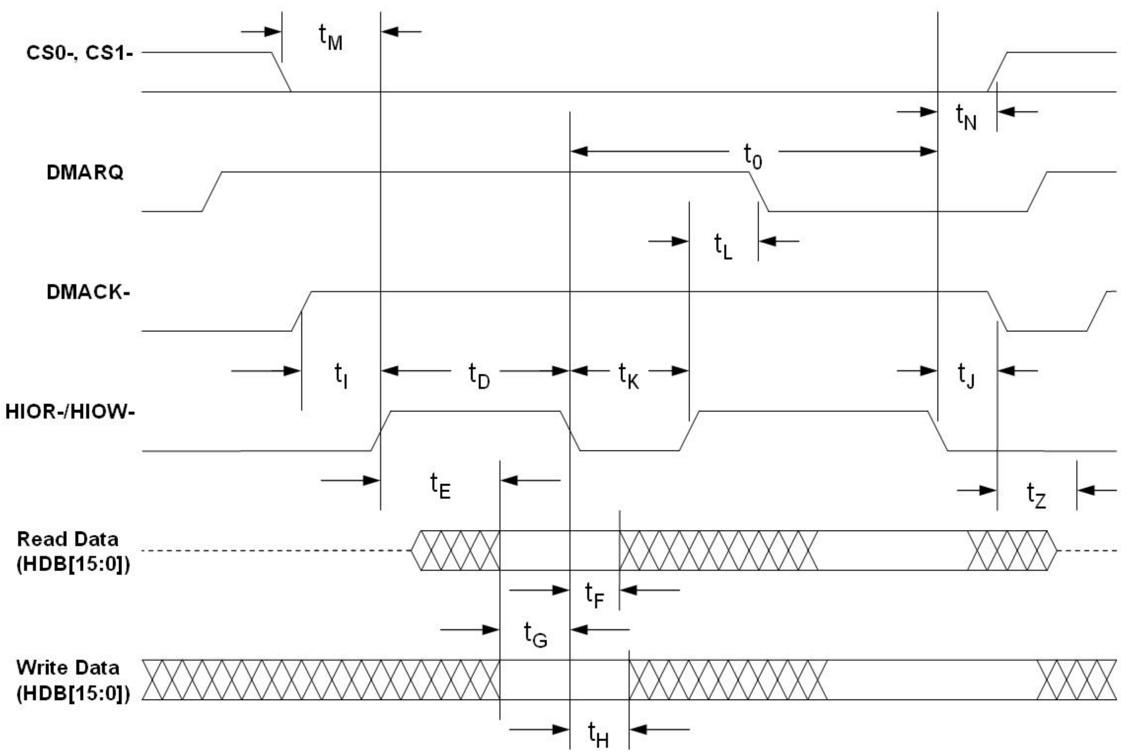

Table 14: Read/Write Timing Specifications, Multiword DMA Mode 0-2

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_0	Cycle time (min.)	480	150	120
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70
t_E	HIOR- data access (max.)	150	60	50
t_F	HIOR- data hold (min.)	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20
t_H	HIOW- data hold (min.)	20	15	10
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25
t_{KW}	HIOW- negated width (min.)	215	50	25
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t_N	CS1-, CS0- hold	15	10	10
t_Z	DMACK-	20	25	25

Ultra DMA mode

Figure 6: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

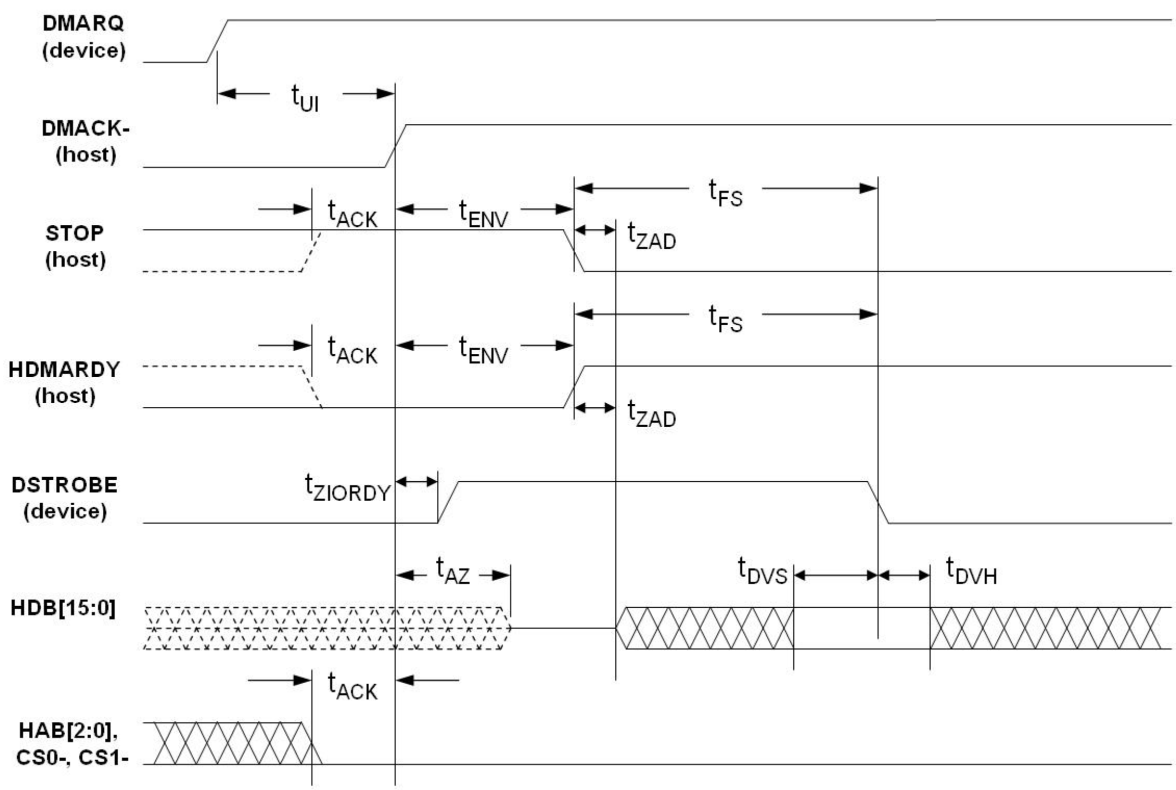

Figure 7: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

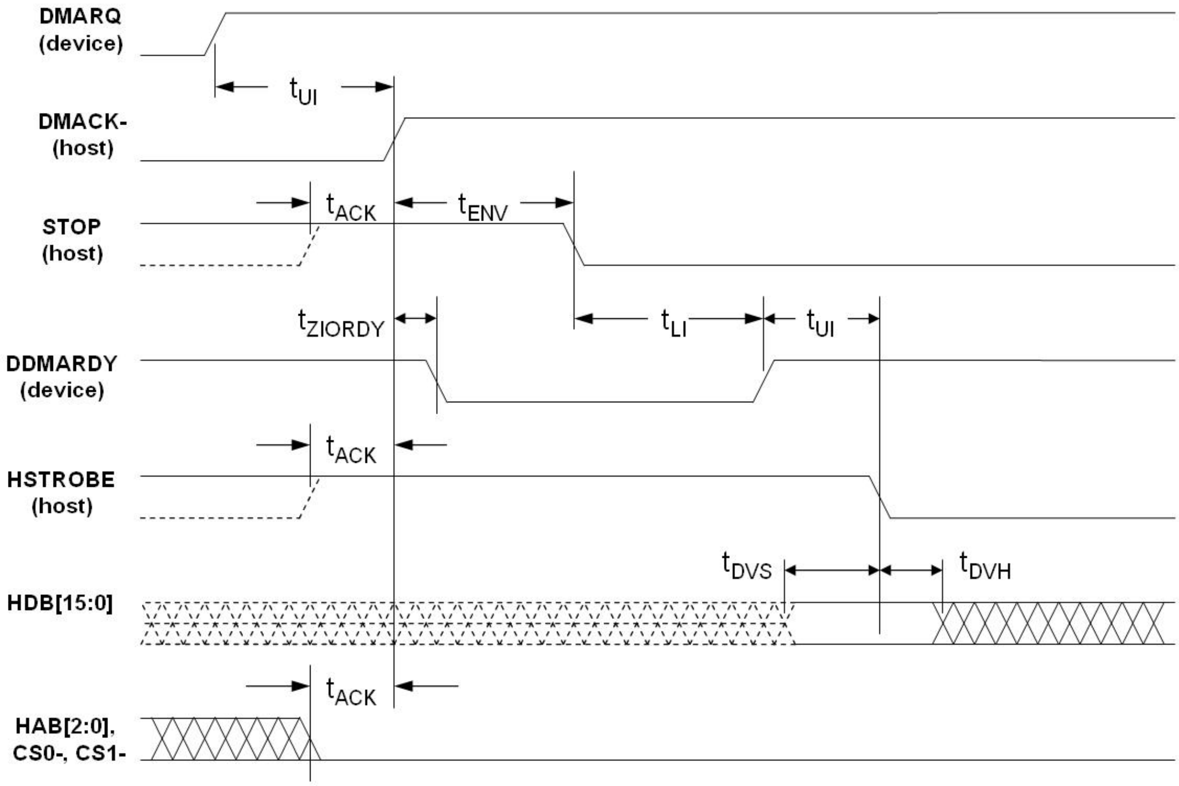

Figure 8: Sustained Ultra DMA Mode Data-in Burst Timing Diagram

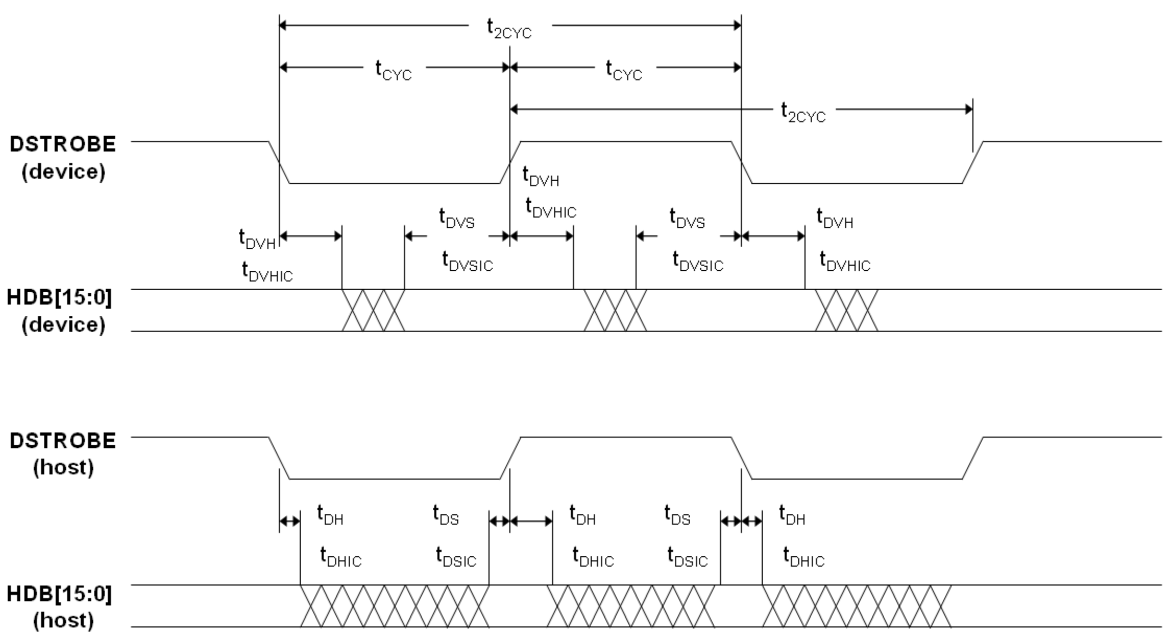

Figure 9: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

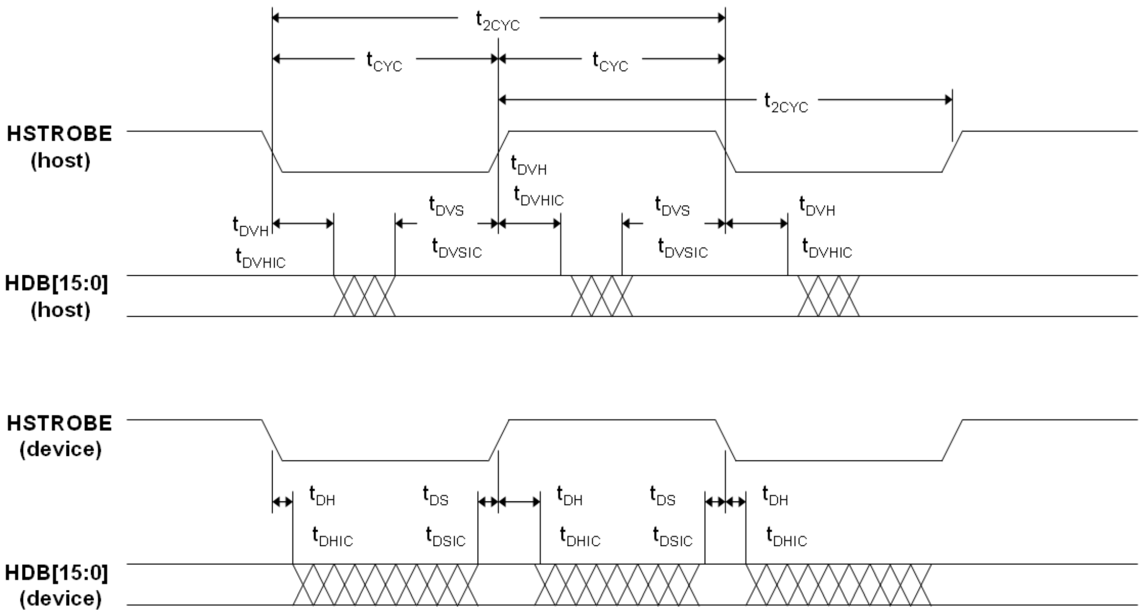

Table 15: Timing Diagram, Ultra DMA Mode 0-4

Ultra DMA timing parameters		**Mode 0**		**Mode 1**		**Mode 2**		**Mode 3**		**Mode 4**	
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	120	-	90	-	60	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	115	-	86	-	57	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	170	-	130	-	120
Ultra DMA timing parameters		**Mode 0**		**Mode 1**		**Mode 2**		**Mode 3**		**Mode 4**	
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
t_{LI}	Limited interlock time	0	150	0	150	0	150	0	100	0	100
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4	
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	20	-	20	-

4. Command Descriptions

4.1. Command Set

The following table summarizes the command defined in ATAPI-6 specification and lists the commands supported by the controller.

Table 16: IDE Commands

Command Name	Command Code
Check Power Mode	98H or E5H
Execute Device Diagnostic	90H
Erase Sector	C0H
Format Track	50H
Identify Device	ECH
Idle	97H or E3H
Idle immediate	95H or E1H
Initialize Device Parameters	91H
NOP	00H
Read Buffer	E4H
Read Long Sector	22H or 23H
Read Multiple	C4H
Read Sector	20H or 21H
Read Verify Sector	40H or 41H
Recalibrate	1XH
Seek	7XH
Set Features	EFH
Set Multiple Mode	C6H
Set Sleep Mode	99H or E6H
Standby	96H or E2H
Standby Immediate	94H or E0H
Write Buffer	E8H
Write Long Sector	32H or 33 H
Write Multiple	C5H
Write Sector	30H or 31H
Write Verify	3CH

5. Installation Procedure

5.1. *Before unpacking*

Before unpacking or handling a drive, take all proper electrostatic discharge (ESD) precautions, including personal and equipment grounding. Before you start to install the 44-pin 2.5” PATA (IDE) SSD into your system – please check the following.

- If the shipping package appears to be damaged or water stained, notify your dealer.
- Remove the disk from its shipping enclosure and inspect it for any damage that may have occurred during shipment. If any damage is observed, notify your dealer.
- Record the disk serial number and shipment date.
- Retain the original shipping enclosure and all packing material for re-shipment.

5.2. *ESD Precautions*

You can prolong the life of your 2.5” PATA (IDE) SSD as well as increase its reliability and prevent unnecessary damage by following the instructions listed below. Failure to follow any of these instructions may void your warranty.

(1) Always take all proper electrostatic discharge (ESD) precautions, including personnel and equipment grounding.

(2) Always operate the SSD within the environmental specifications.

(3) Always use a grounded wrist strap when handling the SSD. Drives that are not installed in the system are sensitive to ESD damage.

5.3. *IDE Device Setup / Auto-Detection*

Most BIOS have an entry in the Standard Setup menu for each of the four IDE/ATA devices supported in a system (primary master, primary slave, secondary master, and secondary slave). For each one, you can enter a value for each setting in this section (type, size, cylinders, etc.).

Virtually all BIOS now come with IDE device Auto-Detection. This comes in two forms:

- **Dynamic IDE Auto-Detection:** This is the fully automatic mode. You set one or more of the IDE devices (primary master, primary slave, etc.) on "Auto" and the BIOS will automatically re-detect and set the correct options for the drive each time you boot the PC. The BIOS will usually display on the screen what device it finds each time it auto-detects. For most people, this is the best way to go; it ensures that your

BIOS always has the correct information about your hardware, and it removes any possibility of you installing a new drive but forgetting to set up the CMOS properly, or of changing a parameter by mistake in the setup program. Not all BIOS offer this setting but most never ones do.

- **Manual IDE Auto-Detection:** This type of Auto-Detection is run from the BIOS setup program. You select Auto-Detection, and the BIOS will scan the IDE channels, and set the IDE parameters based on the devices it finds. When you save the BIOS settings, they are recorded permanently. The disadvantage of this is that if you change devices, you must return to the BIOS to re-auto-detect the new devices (unlike the dynamic Auto-Detection scheme, which does a fresh Auto-Detection each time you boot the PC). Virtually every BIOS created in the last 8 to 10 years offers manual Auto-Detection.

When you use dynamic Auto-Detection, the BIOS will normally "lock" the individual device settings that are being automatically set by the BIOS at boot time. Most systems that provide manual Auto-Detection will *not* lock the individual settings; they auto-detect, set the settings, and then let you change them if you want to. In most cases of course, you will not want to change what the BIOS detects.

Most BIOS that allow dynamic Auto-Detection also allow manual Auto-Detection; the choice is yours. Using some sort of Auto-Detection for IDE/ATA devices is *strongly* recommended. It is the best way to reduce the chances of disk errors due to incorrect BIOS settings. It also provides immediate feedback of problems; if you can't auto-detect a drive from the BIOS, you know you have a problem even before you try to boot up.

5.4. *Partition & Format*

Before you install your operating system, you must first create a primary partition on the 2.5” PATA (IDE) SSD on the system, and then format a file system on that partition. The Fdisk tool is an MS-DOS-based tool that you can use to prepare (partition) the 2.5” PATA (IDE) SSD. You can use the Fdisk tool to create, change, delete, or display current partitions on the 2.5” PATA (IDE) SSD, and then each allocated space on the 2.5” PATA (IDE) SSD (primary partition, extended partition, or logical drive) is assigned a drive letter. Disk 1 may contain one extended partition, and a second 2.5” PATA (IDE) SSD may contain a primary or extended partition. An extended partition may contain one or more logical MS-DOS drives.

After you use the Fdisk tool to partition 2.5” PATA (IDE) SSD, use the Format tool to format those partitions with a file system. The file system File Allocation Table (FAT) allows the 2.5” PATA (IDE) SSD to accept, store, and retrieve data. Windows 95 OEM Service Release 2 (OSR2), Windows 98, Windows 98 Second Edition, Windows Millennium Edition (Me), and Windows 2000 support the FAT16 and FAT32 file systems. When you run the Fdisk tool on a 2.5” PATA (IDE) SSD that is larger than 512 megabytes (MB), you are prompted to choose one of the following file systems:

FAT16: This file system has a maximum of 2 gigabytes (GB) for each allocated space or drive letter. For example, if you use the FAT16 file system and have a 6-GB 2.5” PATA (IDE) SSD, you can have three drive letters (C, D, and E), each with 2 GB of allocated space.

FAT32: This file system supports drives that are up to 2 terabytes in size and stores files on smaller sections of the 2.5” PATA (IDE) SSD than the FAT16 file system does. This results in more free space on the 2.5” PATA

(IDE) SSD. Its file system does not support drives that are smaller than 512 MB.

When you run the **fdisk** and **format** commands, the Master Boot Record (MBR) and file allocation tables are created. The MBR and file allocation tables store the necessary disk geometry that allows 2.5” PATA (IDE) SSD to accept, store, and retrieve data.